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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/626,592	07/25/2003	Takeshi Matsunaga	240900US2S	9746

22850 7590 11/28/2005

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EXAMINER	
FENTY, JESSE A	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 11/28/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H:A

Office Action Summary	Application No.	Applicant(s)	
	10/626,592	MATSUNAGA ET AL.	
	Examiner	Art Unit	
	Jesse A. Fenty	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-13* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 13* is/are rejected.

7)☒ Claim(s) *11, 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *09/14/05*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 102

1. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

2. Claims 1-10 and 13 are rejected under 35 U.S.C. 102(b) as being anticipated by Yeh et al. (U.S. Patent No. 6,294,834 B1).

In re claim 1, Yeh (esp. Fig. 1) discloses a semiconductor device, comprising:

a multilayer wiring structure including a plurality of wiring layers formed on a substrate;

a capacitor arranged in a predetermined wiring layer in the multilayer wiring structure and including a lower electrode (34), a dielectric film (36), and an upper electrode (38);

a first via (layer just above "N3") formed in the predetermined wiring layer and connected (through N3) to a top surface of the upper electrode of the capacitor; and

a second via formed in an overlying wiring layer stacked on the predetermined wiring layer, the second via being formed directly on the first via and the second via being connected to a wiring (52) formed in the overlying wiring layer.

In re claim 2, Yeh discloses the device of claim 1, wherein the first via is formed to have a larger cross section than that of the second via.

In re claims 3 and 4, Yeh discloses the devices of claims 1 and 2 respectively, wherein the predetermined wiring layer has a third via (adjacent the first via) formed on the lower electrode and a wiring connected to the third via and buried in a surface of the predetermined wiring layer.

In re claims 5 and 6, Yeh discloses the devices of claims 3 and 4 respectively, wherein the wiring comprises copper, and a copper diffusion stopper film (40) is formed on the surface of the predetermined wiring layer to prevent diffusion of the copper forming the wiring.

In re claims 7 and 8, Yeh discloses the devices of claims 1 and 2 respectively, wherein the overlying wiring layer has a wiring connected to a top of the second via and buried in a surface of the overlying wiring layer.

In re claims 9 and 10, Yeh discloses the devices of claims 1 and 2, wherein a third via (adjacent the first via) formed on the lower electrode of the capacitor is provided in the predetermined wiring layer;

a fourth via formed connected to a top of the third via and formed to be thinner than the third via is provided in the overlying wiring layer; and

the second and fourth vias are connected to the first (52) and second (56) wirings, respectively, buried in a surface of the overlying wiring layer.

In re claim 13, Yeh (esp. Fig. 1) discloses a semiconductor device, comprising:

at least one impurity diffusion layer (28) formed in a first area of a semiconductor substrate;

a plurality of wiring layers stacked on the semiconductor substrate and including a first wiring layer having a contact connected to the impurity diffusion layer and a first wiring buried in the first wiring layer and connected to the contact;

a capacitor formed in a predetermined one of the plurality of wiring layers which predetermined wiring layer is formed on a second area different from the first area of the semiconductor substrate, the capacitor having a stacked structure of a lower electrode (34), a dielectric film (36), and an upper electrode (38);

a first via (above N3) formed on at least the upper electrode formed in the predetermined wiring layer;

an upper wiring layer having an interlayer insulating film (40) stacked on the predetermined wiring layer, a second via (2^{nd} layer above "N3) formed in the interlayer insulating film, connected to the first via, and formed to be thinner than the first via, and a second wiring (52) connected directly to the second via and buried in a surface portion of the upper wiring layer.

Allowable Subject Matter

3. Claims 11 and 12 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Response to Arguments

4. Applicant's arguments filed 09/14/05 have been fully considered but they are not persuasive.

Applicant argues that the patent of Yeh et al. cannot be used to anticipate the instant claims because "wiring" layers are not analogous to "via" layers.

Applicant cites *Ferguson Beauregard/Logic Controls* for the proposition that "it is the use of the words in the context of the written description and customarily by those skilled in the relevant art that accurately reflects both the 'ordinary' and the 'customary' meaning of the terms in the claims."

In this case, applicant does not cite any specific language in the specification that clearly differentiates a via layer from a wiring layer, as interpreted in the present rejection.

In the present rejection, studying Fig. 1 of Yeh et al., there is no appreciable difference between the structure of the "via" layers (V1 and V2, as denoted by Applicant) and the "wiring" layer (M1). All three layers are metallized plugs of particular sizes, two of the same width, the third of another. Although the knowledge of one skilled in the art can be relied upon for what is "ordinary" and "customary," this standard does not apply "exclusively" to all claim terms.

During examination, the claims must be interpreted as broadly as their terms reasonably allow. *In re American Academy of Science Tech Center*, 2004 WL 1067528 (Fed. Cir. May 13, 2004). In this case, the only positive limitations regarding the first via layers are that such layer is connected to the top electrode and that such layer has a

larger cross-section than the layer directly on top of it. Such limitations are clearly met by the structure of Yeh et al as described in the instant rejection.

Simply labeling different metal plug layers "vias" or "wiring layers" without specifically claiming the structural difference between the layers is analogous to attempting to define a structure by its intended use.

A recitation of the intended use of the claimed invention must result in a structural difference between the claimed invention and the prior art in order to patentably distinguish the claimed invention from the prior art. If the prior art structure is capable of performing the intended use, then it meets the claim.

In this case, the structure of the "via" and the structure of the "wiring layer" are analogous, except for the width of each and the vertical positioning of each. Presented with a stack of metal layers of equal proportions, the labeling of one layer a "via" and another layer a "wiring" is insignificant if the total structure reasonably reads on the claim in question.

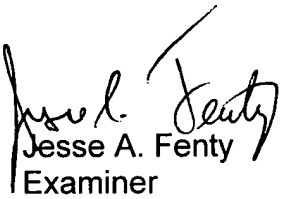
For these reasons, the rejection based on Yet et al. is maintained.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jesse A. Fenty whose telephone number is 571-272-1729. The examiner can normally be reached on 5/4-9 1st Fri. Off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Ken Parker can be reached on 571-272-2298. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Jesse A. Fenty
Examiner
Art Unit 2815